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HOGAN & HARTSON L.L.P.
1999 AVENUE OF THE STARS
SUITE 1400
LOS ANGELES, CA 90067

EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,582	MATSUMOTO, KENJI	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it is over 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 7 and 13 state "a scanning-line driving circuit that sequentially selects the plurality of scanning lines one by one" or "sequential selecting the plurality of scanning lines one by one by a scanning line driving circuit", but then they state "wherein the control section that controls the light emission time of the optical elements by a non-sequential scanning operation that selects a scanning line in a discontinuous order against an arranged order of the scanning lines" or "controlling the light emission time of the optical elements by a non-sequential scanning operation that selects a

scanning line in a discontinuous order against an arranged order of the scanning lines". Thus, how can the line be sequentially selected one by one and also be non-sequentially selected in a discontinuous order. Therefore, it is unclear the intention of the claims.

For examination purposes, the examiner will assume that the lines are selected non-sequentially, as that is the invention described in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-2, 7-8 and 13-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda et al. (US 2002/0057242) in view of Yakamura et al. (JP 2002-049361).

Regarding claim 1, Yoneda et al. disclose an image display system, comprising:

an image processing device (Figure 2, items 135, 136 and 137); and

an electro-optic apparatus, comprising:

a pixel matrix, where pixels including optical elements are arranged in a matrix shape (Figure 2, LR1-C1 through LRm-Cn contain optical elements. See paragraph [0050].);

a plurality of scanning lines coupled to a pixel group arranged along either one of a row direction or a column direction of the pixel matrix (Figure 2, R1-Rm);

a plurality of data lines coupled to the pixel group arranged along either one of the row direction or the column direction of the pixel matrix (Figure 2, C1-Cn);

a scanning-line driving circuit that sequentially selects the plurality of scanning lines one by one (Figure 2, item 131);

a data-line driving circuit that outputs a control signal related to light emission of the optical elements to, at least, one data line of the plurality of data lines (Figure 2, item 132);

a control section that controls an operation of the scanning-line driving circuit and the data-line driving circuit (Figure 2, items 133 and 134); and

an input image data acquisition section that obtains input image data transmitted from the image processing device (Figure 2, item 134 obtains the image information from the image memory 137.),

wherein the image processing device generates the input image data to be inputted into the electro-optic apparatus and transmits the input image data to the electro-optic apparatus (Figure 2, item 136 sends the input image data to the image memory 137 which then inputs the image data to the circuit 134 of the electro-optic device.), and

wherein the control section that controls the light emission time of the optical elements by a non-sequential scanning operation that selects a scanning line in a discontinuous order against an arranged order of the scanning lines, and gradationally displays an input image on a display area defined by a predetermined number of the scanning lines and the data lines (Paragraph [0052] and paragraphs [0090]-[0117]).

Yoneda et al. fail to explicitly teach that the control section that controls the light emission time of the optical elements by a non-sequential scanning operation that selects a scanning line in a discontinuous order against an arranged order of the scanning lines, based on gradation data of a predetermined bit length corresponding to the input image data and a number of light emission gradation of the optical elements.

Yakamura et al. disclose an image display system wherein a control section controls the light emission time of the optical elements by a non-sequential scanning operation that selects a scanning line in a discontinuous order against an arranged order of the scanning lines, based on gradation data of a predetermined bit length corresponding to the input image data and a number of light emission gradation of the optical elements (Paragraph [0016] and Drawing 10).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teachings of Yakamura et al. of arranging the scanning line order based on gradation data in the image display system taught by Yoneda et al. in order to stabilize the display and reduce flicker.

Regarding claim 7, this claim is rejected under the same rationale as claim 1.

Regarding claim 13, this claim is rejected under the same rationale as claim 1.

Regarding claims 2 and 8, Yoneda et al. and Yakamura et al. disclose the image display system according to claims 1 and 7.

Yoneda et al. also disclose wherein a predetermined amount of pixel data, with a rearrangement that has been completed, is transmitted to the electro-optic apparatus every time the rearrangement has been completed (Paragraphs [0093] and Figures 3 and 4, where it is inherent that image data and scanning line drive signals will be supplied each time the scanning lines are to be scanned, i.e. every time the "rearrangement" is completed.).

Regarding claim 14, Yoneda et al. and Yakamura et al. disclose the method according to claim 13.

Yakamura et al. also disclose the method further comprising:

obtaining a bit length N of the gradation data indicating the light emission gradation of the optical elements and a numerical group obtained by dividing an added number, obtained by adding one to a-total number of the scanning lines, with a proportion comprising 2^n values (n= 0, 1 and 2 through (N- 1)) of a number of bits in a bit string constituting the gradation data; and associating a serial number to each of the scanning lines with the arranged order of the scanning lines (Paragraphs [0009]-[0010] explains that numbers associated with the scanning order are assigned to the different scanning lines, where the scanning liens are divided into groups and the bit length of the data is known , i.e. the number of subfields.).

Regarding claim 15, Yoneda et al. and Yakamura et al. disclose the method according to claim 14.

Yakamura et al. also disclose the method further comprising:

assigning a predetermined number of the serial numbers, which have been associated to the scanning lines, as an initial value corresponding to a least significant bit (0th digit) of the bit string constituting the gradation data (Paragraphs [0010] and [0016] and Drawing 10 explain that numbers indicating the order are assigned to the scanning lines corresponding to the lower bit, see Drawing 10(a) where from t= to t=5H the line 0, 15, 13 , 9 and 1 are selected in that order.); and

assigning a number, obtained by adding a largest number contained in the numerical group to the initial value corresponding to the least significant bit, as the initial value of the scanning line corresponding to a most significant bit ((N-1) digit) of the bit

string constituting the gradation data (Paragraph [0010] and [0016] and Drawing 10 explain that line 9 is assigned the initial value of the scanning line with SF4.).

Regarding claim 16, Yoneda et al. and Yakamura et al. disclose the method according to claim 15.

Yakamura et al. also disclose the method further comprising associating an added value, obtained by adding one to a bit-digit of another bit from a lower bit-digit, as an initial value of the other bit, out of the initial value corresponding to one digit higher than bit digit of the other bit and the numerical values contained in the numerical group, sequentially from the higher bit-digit of the other bits, concerning the other bits between the most significant bit and the least significant bit (Paragraph [0010] and [0016] and Drawing 10 explain that line 13 is used for SF3 and line 15 is used for SF2.).

Regarding claim 17, Yoneda et al. and Yakamura et al. disclose the method according to claim 16.

Yakamura et al. also disclose the method further comprising a first processing that selects the scanning line of the serial number indicated by the initial value corresponding to the least significant bit at first, and sequentially selects each of the scanning line of the serial number indicated by the initial values corresponding to the most significant bit and each bit, which is shifted bit by bit from the most significant bit towards the bit before the least significant bit (Paragraph [0010] and [0016] and Drawing 10(b) show that lines 0, 15, 13 and 9 are selected in that order.).

Regarding claim 18, Yoneda et al. and Yakamura et al. disclose the method according to claim 17, further comprising a second processing that makes the scanning-line driving circuit drive the scanning line of the selected number every time the scanning line is selected (It is inherent that the scanning line drive circuit will drive the scanning lines when they are to be selected.).

Regarding claim 19, Yoneda et al. and Yakamura et al. disclose the method according to claim 18.

Yoneda et al. also disclose the method further comprising a third processing that adds one to a value that has been associated with each bit of the gradation data, respectively, while if the value corresponding to each bit of the gradation data after the addition exceeds the value, obtained by subtracting one from the total number of the scanning lines, the process updates the value to the minimum value of the serial number (Paragraphs [0012]-[0016]).

Regarding claim 20, Yoneda et al. and Yakamura et al. disclose the method according to claim 19.

Yakamura et al. also disclose the method further comprising a fourth processing that selects the scanning line, corresponding to the value that has been associated to each bit of the gradation data after the third processing, with the same sequence of the first processing, wherein a control program for the image processing device determines

the selection order of the scanning lines by repeating the second processing through the fourth processing until all the scanning lines on the display area have been selected for each bit of the bit string constituting the gradation data, and generates the input image data based on the determined selection order (Drawing 10(a) shows that the scanning lines are selected for each of SF1 through SF4 until all of the scanning lines are selected, where the input image data is generated corresponding to the order of selection.).

7. Claims 3-6 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda et al. (US 2002/0057242) in view of Yakamura et al. (JP 2002-049361)and further in view of Katakura et al. (JP 05-127629).

Regarding claims 3 and 9, Yoneda et al. disclose the image display system according to claims 1 and 7.

Yoneda et al. fail to explicitly teach wherein the image processing device comprises: an input image data generation section, a frame memory, and an input image data transmission section.

Katakura et al. disclose of an image processing device (Drawing 1, item 102) that comprises:

an input image data generation section (Drawing 1, item 113),

a frame memory (Drawing 1, item 114), and

an input image data transmission section (Drawing 1, item 112).

Therefore, because both Yoneda et al. and Katakura et al. both teach of image processing devices for use with a display, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to substitute one image processing device for the other to achieve the predictable result of processing an image.

Regarding claims 4 and 10, Yoneda et al. and Katakura et al. disclose the image display system according to claims 3 and 9.

Yoneda et al. and Katakura et al. fail to explicitly teach wherein the input image data generation section carries out image processing obtained from a personal computer to generation the input image data, however, since it is not disclosed in the specification that this is essential to the invention, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made for the image display system to receive input image data from a computer in order to provide a display for the computer such that the computer would be usable.

Regarding claims 5 and 11, Yoneda et al. and Katakura et al. disclose the image display system according to claim 4s and 10, wherein the input image data is rearranged according a selection order of the scanning lines by the non-sequential scanning operation in the electro-optic apparatus (As described above, Yoneda et al. discloses that the scanning lines are scanned in a discontinuous order so as to create

the display, which inherently means that the input image data will be arranged according to the selection or else the display would not work.,).

Regarding claims 6 and 12, Yoneda et al. and Katakura et al. disclose the image display system according to claims 3 and 9.

Katakura et al. also disclose wherein the frame memory includes two storage regions (Paragraph [0024]).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

25 January 2008

AMR A. AWAD
SUPERVISORY PATENT EXAMINER